

## **3D. Innovation on the Shopfloor: Successes from the Semiconductor Industry**

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### **3D.1 Introduction**

In this paper, we focus on shop floor innovation and problem-solving activities in semiconductor manufacturing. Through an analysis of firm-level data from Asia, Europe and the U.S., this paper demonstrates how semiconductor companies have structured their employment systems to solve the technically demanding problems that arise daily on the shop floor.

We explore the following hypothesis: *In a high-tech environment, key ingredients of a high performing human resource (HR) system include:*

- *incentives for creativity and systems for control in managing innovation by engineers;*
- *the organization of work so that line workers develop and use problem-solving skills;*
- *team problem solving and the sharing of knowledge across all job categories; and*
- *the formation of career ladders so that skill development, responsibilities, and compensation are linked over a worker's tenure.*

Innovation can be divided into two fairly distinct activities in terms of when and where the innovation occurs. One type of innovation occurs during the development of a new product or process, and the second type occurs through follow-on improvements on the shop floor. Long-run competitiveness of a leading-edge company depends on its product line, while short-run competitiveness depends on price and reliability. The challenge for an industry leader is to bring a new product to market as dictated by its long-run product plan and recoup development costs during the short period when competition is limited and prices are relatively high. An industry follower must enter the market with a comparable product at a low cost, since the entry of competitors (followers) into the market causes prices to drop rapidly. This type of price competition drives shop floor innovation, which influences the cost and quality of the product.

The success of a semiconductor process flow depends critically on engineering talent—both of the design and development engineers who craft the process and of the manufacturing engineers who maintain it in a high-volume setting. Engineering expertise guides the complex problem-solving activities during the introduction of a new process as well as continuous improvement projects for mature processes. Because of the technical complexity associated with circuit design and the integration of process steps, operators

and technicians are constrained in their ability to solve technical problems without formal training in engineering. Consequently, operators and technicians have limited involvement in new process introduction, but they participate in solving both one-time and recurring problems with installed processes, usually operating in teams with engineers. We first analyze how shop floor innovation by engineers is controlled and rewarded (Section 3D.2). Through a comparison of practices followed by a Japanese company and a U.S. company, striking differences in the control of engineers' creativity emerge.

In Section 3D.3, we examine the participation of operators, technicians as well as engineers in two primary problem-solving activities—equipment maintenance and statistical process control (SPC). Using fieldwork and survey data,<sup>2</sup> we analyze how the participation of each job category in equipment maintenance and SPC correlates with five performance metrics: defect density, stepper throughput (an indication of equipment utilization), line yield, cycle time, and direct labor productivity. These correlations demonstrate the importance of both engineering involvement in day-to-day problem solving and the integration of line workers into problem-solving activities.

To explore the role of knowledge sharing that occurs on the shop floor, we next analyze data on how firms structure group problem solving (Section 3D.4). Our results suggest that a semiconductor company's need to solve problems quickly and permanently requires that operators and technicians identify problems immediately and then work with engineers to uncover root causes and implement lasting solutions. Engineers guide the process of problem solving and innovation and use technicians, and operators to a lesser extent, as assistants.

The structure of team activities does not distinguish the companies in our sample; instead, how the teams execute problem solving influences success. Drawing from our field work with the CSM team, we present examples of effective problem solving in Section 3D.5. At most fabrication facilities (fabs) that we visited, engineers, technicians, and operators all participate in problem-solving activities commensurate with their technical training. We present examples of advanced problem solving undertaken in Japan, Korea, and the United States.

In Section 3D.6, we inspect the development of problem-solving skills through work organization and career ladders. We provide an overview of training in the semiconductor industry and discuss task allocation across job categories. We also illustrate examples of career ladders for semiconductor line workers in the U.S. and Japan. The U.S. semiconductor industry has very few unionized fabrication facilities, so although semiconductor line workers perform relatively high-skilled tasks, they earn substantially less than UAW production and craft workers in the U.S. In the final section (Section 3D.7), we summarize the key components of a high performing HR system in a technology-intensive industry.

## **3D.2 Engineering Innovations on the Shopfloor**

Successful innovation requires both creativity and control. For the purposes of this research, we define creativity as the generation of new ideas and departures from past practices in the manufacturing process. The need for control over creativity is crucial while innovating in the semiconductor industry, since the individual steps of the manufacturing process are highly interdependent and products have a large number of characteristics that must be within critical limits and are costly to measure and test. Often the two forces of creativity and control are in conflict, and a successful management system must negotiate the tension between them. In this section, we document and analyze examples of how these tensions are adeptly managed at a leading Japanese producer of memory chips (pseudonym “JapanTech”) and a leading American producer of logic chips (pseudonym “USTech”).<sup>3</sup>

In managing engineers’ creativity, two major tensions must be addressed:

- preventing unauthorized changes to the production process by engineers while keeping them actively involved in suggesting improvements;
- having manufacturing engineers remain engaged in less interesting, but necessary, tasks rather than doing more challenging activities that are not part of their assignment.

The management of creativity and control operates through different environments in Japan compared to the U.S. Here we will mention the role of education and wage-setting institutions. The educational system and its link to industry creates important differences in the skill development process. USTech’s engineers specialize in development (advanced degrees) and fabrication activities (B.S. degree). When USTech hires research engineers with advanced degrees and manufacturing engineers with B.S. degrees, often straight out of the university, they are assumed to have the research skills necessary to undertake their own research projects or the manufacturing skills necessary to oversee the operation of specific equipment, respectively. At JapanTech, both research and manufacturing engineers are hired after graduating with a B.S. degree. They are expected to learn on the job through their team work (often from a mentor), continual firm-based training, and job rotation that usually includes both development and fabrication activities. Some engineers earn advanced degrees while employed, either from the company or from an affiliated university.

Since large firms in Japan have similar compensation systems that are largely structured for the junior engineers through negotiations with the union in national annual wage bargaining and through widespread national practices, much of what we observed at JapanTech is representative of other large Japanese electronics companies. In the U.S., few electronics companies have any union representation, and employment practices vary more widely across companies than in Japan. Therefore, USTech’s employment system cannot necessarily be thought of as representative of other large U.S. semiconductor companies.<sup>4</sup> We will indicate which practices are widespread and which seem to be idiosyncratic.

Management of innovation on the shop floor includes ensuring that shop floor improvements are controlled and, with approval, become part of the organization's knowledge base. In semiconductors, the consequences of modifications that are not standardized or approved can be serious, since the characteristics of the chip may be affected inadvertently. Making unauthorized modifications is often referred to as "tweaking" the process. However, JapanTech and USTech differ in their approaches to controlling process tweaks, which reflect their timing of and their procedures governing the transfer of a new product to manufacturing.

### ***3D.2a Exact replication and problem solving at USTech***

USTech has adopted a strategy that ties short-run activities to long-run planning as they transfer process technology across fabs. USTech takes extreme measures to ensure that the fabrication process is replicated exactly when it is transferred between its plants and that any potential improvement goes through appropriate channels before being implemented. USTech instituted the rule of *exact replication* of process specifications in order to minimize portability problems and eliminate declines in yields over time. This rule was adopted after USTech experienced declines in yield following transfers of new processes from development sites to high-volume fabrication facilities (fabs). In previous experiences, when the new process technology was transferred to high volume, the manufacturing engineers would modify the process in order to solve manufacturing problems, and the yield would fall. As one manager said, "We had to crush creativity in manufacturing fabs (no tweaking). We start with top down control, and fabs need approval for any changes."

To improve compliance by the manufacturing engineers to the exact replication rule, many of them are temporarily transferred to the development plant ahead of the process transfer. They assist the development engineers in finalizing the characterization of the process. By the time of transfer to the high-volume fab, manufacturing engineers have assumed ownership. As one USTech manager said, "We are trying to combine the development skills of the development engineer with problem-solving skills of the manufacturing engineer" by having the development and manufacturing engineers overlap prior to process transfer.

Prohibiting manufacturing engineers from making unauthorized improvements in the process reflects the differences in educational and skill requirements of engineers in development versus manufacturing (fabrication). The restriction also underscores the sophisticated nature of the technology and the difficulty in qualifying a logic chip's characteristics to meet customer requirements following process modification. In contrast to USTech, other U.S. semiconductor companies transfer a less mature process from development to their high-volume fabs and allow more improvements as well as modification of existing equipment at the fabrication plant. USTech's exact replication is a costly strategy, which precludes widespread adoption by other U.S. producers.

Exact replication reduces the scope of problem solving at the manufacturing site, but the transfer process remains a challenge. Exact replication can only be a relative

concept, since variations in the process occur as volume increases. One manager said, “Exact replication needs common sense: how to measure, and who decides. We want the fab to copy exactly and then get help with problems. This requires a lot of training for engineers in the manufacturing fab.” The formal methodology for the hand-off from development to manufacturing includes using and updating a rule book, which gives processing specifications, information on running equipment modules, and baseline performance. The rule book is not comprehensive, but interpretive. It should be “a living document” with engineers adding approved information as the production volume increases. However, as one manager explained, “Engineers do not like to document, and so updates are hard to get done. They don’t have a customer, so the incentive is gone.”

So management must discourage tweaking, and encourage the more mundane but necessary tasks, such as writing up the documentation for process changes and calibrating equipment. The engineers would rather be doing the more challenging tasks of troubleshooting out-of-control process steps, which may not be part of their assignment. As discussed in subsequent sections, successful outcomes in semiconductor manufacturing require engineering leadership and guidance, even in mundane activities.

### ***3D.2b Making improvements and solving problems at JapanTech***

JapanTech is a conglomeration of many fabs that operate as separate companies with different cultures. The parent R&D center must decide how much power to give the fabs in order to motivate and encourage creativity while maintaining control. The manufacturing engineers at the fabs must be made to feel like they are part of the parent company while at the same time they strive to make their fab outstanding. JapanTech encourages competition among its plants on cost performance and on improvements or refinements to the system. Each year JapanTech sets target goals for prices and costs and highlights the fab showing the best performance. Competition is more spiritual than monetary; as noted by one JapanTech manager, “Japanese don’t want to lose.” Yet to ensure successful process introductions, JapanTech must encourage cooperation between engineers from the parent company and the plants, and among engineers from different plants. Communication among engineers is an important part of coordination across division and plants. Production processes often are transferred to more than one plant. The first high-volume fab to receive the process becomes the source fab for the next plant to receive the process. Often the second recipient fab has older equipment but is expected to achieve the same yields. Since the fabs are in competition, this may affect their cooperation in making the transfer.

In contrast to USTech’s strategy, JapanTech’s development lab does *not* undertake activities involved in developing the commercial samples of its new chips. These activities (*e.g.*, improve process and equipment to get reasonable yield, confirm device reliability, and complete qualification samples) are done at the mass production fab. Generally, JapanTech purchases only 20% new equipment for volume production at the receiving fab. For the rest of the equipment, the development fab issues specifications and the manufacturing engineers modify the existing equipment. This is in stark contrast to USTech’s exact replication policy which requires that the equipment sets match.

JapanTech's strategy is to make many products on the same line, which adds depth of knowledge that facilitates the manufacture of multiple variations for a particular product line. This approach is consistent with JapanTech's reliance on teamwork and group responsibility with engineers engaging in a broad range of job tasks. Since engineers' skills are largely developed through company-based classes, mentoring, and job rotation, compensation reflects specific career ladders rather than company or individual performance, although individual performance has some impact on speed of promotion.

Similar to USTech, JapanTech brings high-volume fab engineers to the development center so that they understand the process and feel some ownership. The development engineers are loaned by the development center to the high-volume fab during process transfer. Eventually the fab engineers take over the tasks being done by the development engineers. To facilitate process transfer, there are formal meetings attended by engineers and managers, meetings with only engineers, and informal meetings, phone calls, and the exchange of data between the development engineers and the manufacturing engineers. The engineers at the manufacturing fab may suggest changes and send information about suggested refinements to the R&D center.

In summary, USTech's employment system distinguishes between development and manufacturing engineers and is geared toward supporting and rewarding individual creativity in development but not manufacturing. At JapanTech, development and manufacturing activities are less sharply divided for engineers, and the employment system is geared toward supporting and rewarding the group. At USTech, junior development engineers are given major responsibility for developing new technologies. At JapanTech, major assignments are given to subteams, and new ideas are evaluated by a test group. Junior engineers are assigned to work with senior engineers and are expected to learn through their work assignments. At USTech, engineers are rewarded for their individual performance by their next job assignment and level of responsibility, while job assignments in Japan reflect the needs of the group as well as the experience (seniority) of the members. Both companies use a relative performance ranking system to evaluate their engineers, but the rewards for performance are different. Pay, especially for the first dozen or so years while the engineer is in the company union, is more rigidly set at JapanTech than USTech, which is more individual- and company-performance oriented. USTech focuses on rewarding an individual's ideas and efforts. Although both companies pay bonuses, the bonus at JapanTech mainly reflects national wage setting while the bonus at USTech reflects performance at the unit, division, and company levels. Also, USTech engineers can be richly rewarded with stock options.

### **3D.3 Problem-solving Activities Across Job Categories**

Rapid and effective problem solving is a critical activity in the semiconductor industry. While most pronounced in the engineering ranks, the challenge of encouraging creativity in problem solving while maintaining control over the production process extends through all levels of the organization. This section examines the integration of problem-solving activities into the job tasks of operators and technicians as well as

engineers. Since both equipment maintenance and statistical process control (SPC) are central to effective problem solving in a fab, we hypothesize that fabs engaging in technical tasks most intensively should exhibit the highest performance. Using data from the CSM project collected from fifteen fabs in Japan, Europe, and the US, we examine this hypothesis by determining whether manufacturing performance is correlated with equipment maintenance and SPC. The correlations between our quality performance measures (defect density and line yield) and total fab SPC support this hypothesis, although the correlations involving equipment maintenance do not. We also hypothesize that fabs that include their “front-line of defense,” namely their operators and technicians, in equipment maintenance and SPC achieve a higher level of performance. Evidence in support of this hypothesis is found for operators. The data also highlight that process engineers play a vital role in successful SPC activities. A fab’s need to solve problems quickly and permanently requires operators and technicians to identify problems immediately and then work with engineers to uncover root causes and implement lasting solutions.

### ***3D.3a Equipment maintenance***

This section, in concert with Section 3D.3b, probes more deeply into the specific responsibilities for each occupation. This section focuses on equipment maintenance responsibilities, and Section 3D.3b examines SPC activities. Equipment that is chronically down, dirty, or out-of-alignment can prevent world class manufacturing performance, and equipment maintenance activities should be a necessary but not sufficient factor for high performance. The correlations between the level of participation in equipment maintenance across occupations and the five performance metrics show mixed results. The positive correlations for the operator job category support our hypothesis that involving line workers in problem solving can heighten performance.

Figures 3D-1 through 3D-4 demonstrate, as expected, that *technicians* and *equipment engineers* shoulder the greatest level of responsibility when it comes to equipment maintenance and troubleshooting. The charts depict the weighted scores for each equipment maintenance activity summed across all fabs for each job category. (See Appendix 1 for complete descriptions of each activity.) The scores were weighted as follows: High=3, Some=1, None=0. Since fourteen fabs responded to this question for all job categories, the maximum score per activity per job category is 42. Although operators do not play an extensive role in either long-term maintenance or modifications, they are in intimate contact with the equipment—recognizing and documenting abnormalities, cleaning and/or lubricating the equipment, and performing daily or weekly inspections.

To capture the variation across fabs in terms of their use of equipment maintenance activities, we grouped the activities in our survey according to their degree of difficulty as shown in Appendix 1. Then, for three occupations—operator, technician, and equipment engineer—we derived scores for each fab by:

1. weighting each equipment activity according to Appendix 1 (High-Level=3, Medium-Level=2, Low-Level=1);

2. then, multiplying the scores from (1) by weights based on the fab's response (High=3, Some=1, None=0) for each activity;
3. and finally, summing together the double-weighted scores from (2) for the thirty equipment maintenance activities for each occupation for each fab. [Therefore, the maximum score a fab could achieve for one job category is 204: 15 (High score on the 5 Low-Level activities) + 72 (High score on the 12 Medium-Level activities) + 117 (High score on the 13 High-Level activities).] The resulting scores for operators, technicians, and equipment engineers at each fab can be found in Figures 3D-5, 3D-6, and 3D-7, respectively.

No common pattern of substitution between the maintenance activities of technicians and engineers is apparent. As shown by the striped bars in Figure 3D-6, the fabs with the highest equipment maintenance scores for technicians are located in Asia, Europe, and the U.S. As shown by Figure 3D-7, two of the top three in the technician chart remain in the top five and two fall to the bottom four in the corresponding chart for equipment engineers.

Table 3D-1 presents the correlations between the performance metrics and the three occupations. Consistent with our hypothesis that the involvement of line workers in equipment maintenance is important, operator involvement is positively related to line yield performance. Surprisingly the level of technician involvement is not significantly correlated with higher performance.

**Table 3D-1. Equipment Maintenance and Fab Performance Ranking by Occupation**

<b>Performance Metric (Ranking)</b>	<b>Correlation with:</b>		
	<b>Operator Eq. Maint.</b>	<b>Technician Eq. Maint.</b>	<b>Eq. Engineer Eq. Maint.</b>
Defect Density (dd_pcout)	0.26	0.034	-0.065
Stepper Throughput (wopd_out)	0.28	-0.23	0.22
Line Yield (lyd_pout)	0.61**	-0.14	-0.28
Cycle Time (ctpl_out)	0.41	0.017	-0.16
Direct Labor Productivity (dlp_pout)	0.21	-0.089	0.032

\*\*Statistically significant at the 5% level.

Finally, we calculated an “overall” equipment maintenance score for each fab by summing a fab's scores for three occupations: operator, technician, and equipment engineer. These “overall” scores for the fabs are found in Figure 3D-8.

The correlations between the rankings of the fabs from Figure 3D-8 and their rankings for the five performance metrics are presented in Table 3D-2. Although a number

of the correlations between the use of equipment maintenance and performance are negative, none of the correlations is statistically significant.

**Table 3D-2. Equipment Maintenance and Fab Performance Ranking**

<b>Performance Metric (Ranking)</b>	<b>Correlation with Equipment Maintenance</b>
Defect Density (dd_pcout)	0.0022
Stepper Throughput (wopd_out)	-0.083
Line Yield (lyd_pout)	-0.17
Cycle Time (ctpl_out)	-0.033
Direct Labor Productivity (dlp_pout)	-0.12

**3D.3b Statistical process control**

The charts depicting employee involvement in SPC show a similar pattern as those for equipment maintenance (Figures 3D-9 - 3D-12): The tasks performed by the operators and technicians overlap to some degree with the engineers’ tasks (*e.g.*, creating X-bar, R charts), but in many areas, they are complementary (*e.g.*, operators and technicians enter quality data about the process flow into the computer and the engineers use the data for problem identification). In Figures 3D-9 through 3D-12, the example of a “shared task,” creating X-bar, R charts, is shaded gray and the examples of “complementary tasks” are striped. In constructing Figures 3D-9 - 3D-12, the same weighting scheme as described for Figures 3D-1 - 3D-4 was used. The maximum possible score for each SPC activity varies across the job categories according to the total number of fabs that responded. The maximum possible scores are as follows: 42, 45, 42, and 39 for the operator, technician, process engineer, and equipment engineer job categories respectively. Of the three occupations, process engineers are clearly the most involved in advanced problem solving.

In a similar exercise as described above for equipment maintenance activities, we grouped together the SPC activities in our survey in order to calculate the intensity of SPC-use at the fabs. The groupings are presented in Appendix 2. Then, for three occupations—operator, technician, and process engineer—we derived scores for each fab by the same double weighting scheme as described above: We weighted both the fabs’ responses as to the level of participation of each occupation in the activity (High=3, Some=1, None=0), as well as weighting the activity for its degree of difficulty (High-Level=3, Medium-Level=2, Low-Level=1). We then summed together the weighted scores for the eighteen SPC activities to calculate the SPC score for each occupation for each fab. [The maximum score a fab could achieve for one job category is 114: 18 (High score on the 6 Low-Level activities) + 24 (High score on the 4 Medium-Level activities) + 72 (High score on the 8 High-Level activities).] The resulting scores for operators, technicians, and process engineers can be found in Figures 3D-13, 3D-14, and 3D-15, respectively.

As found for equipment maintenance activities, fabs vary in their use of line workers. SPC activities by process engineers are positively and significantly related to efficiency and quality performance metrics (Table 3D-3). Operator involvement in SPC is also positively correlated with quality measures (defect density and line yield), but

negatively related to stepper throughput. However, fabs also vary in their use of SPC activities, and there is no apparent trade-off between the use of operators and engineers in SPC activities.

**Table 3D-3. SPC and Fab Performance Ranking by Occupation**

Performance Metric (Ranking)	Correlation with:		
	Operator SPC	Technician SPC	Process Engineer SPC
Defect Density (dd_pcout)	0.67**	0.45	0.66**
Stepper Throughput (wopd_out)	-0.54*	-0.30	0.54*
Line Yield (lyd_pout)	0.60**	0.40	0.53*
Cycle Time (ctpl_out)	-0.041	-0.13	0.44
Direct Labor Productivity (dlp_pout)	0.18	0.0062	0.74***

\*Statistically significant at the 10% level.

\*\*Statistically significant at the 5% level.

\*\*\*Statistically significant at the 1% level.

Finally, we calculated an “overall” SPC score for each fab by summing together the scores for three occupations: operator, technician, and process engineer. These “overall” SPC scores for the fabs are found in Figure 3D-16. As presented in Table 3D-4, the intensity of SPC activities is correlated with quality measures.

**Table 3D-4. SPC and Fab Performance Ranking**

Performance Metric (Ranking)	Correlation with Fab SPC Ranking
Defect Density (dd_pcout)	0.68***
Stepper Throughput (wopd_out)	-0.29
Line Yield (lyd_pout)	0.52*
Cycle Time (ctpl_out)	-0.16
Direct Labor Productivity (dlp_pout)	0.18

\*Statistically significant at the 10% level.

\*\*\*Statistically significant at the 1% level.

### 3D.4 Team Problem Solving and Intrafirm Knowledge Diffusion

The previous section presented only limited evidence linking problem-solving activities by individuals in particular job categories with fab performance. Effective execution of these activities may require extensive cross-occupational cooperation. Cooperation entails knowledge sharing across job categories and team problem solving.

#### 3D.4a Results from CSM-HR survey

By examining the workings of teams in the fabs in the CSM-HR sample, we documented the structure of group problem solving. Teamwork is commonplace in the majority of fabs in our sample, and teams at different fabs share many characteristics.

Fourteen of the fifteen fabs in our sample reported having at least one of the following types of teams: Quality Improvement Teams/Quality Circles (QITs/QCs), Self-Directed Work Teams (SDWTs), or Cross-Functional Teams (CFTs). Table 3D-5 lists the fabs in our sample and their types of teams. Although many fabs have instituted group problem-solving activities, our interviews with teams during site visits taught us that the level of effectiveness varies greatly.

**Table 3D-5. Presence of Teams**

	Team		
	QIT/QC	SDWT	CFT
1) Fabs in Asia	X		X
AS1	X		
AS2	X	X	
AS3			
AS4	X		X
AS5	X		
AS6	X		
2) Fabs in the U.S.	X	X	X
US1			
US2	X	X	X
US3	X		X
US4	X	X	X
US5		X	X
US6	X	X	X
3) Fabs in Europe	X		X
EU1			
EU2			X
EU3			X

Table 3D-6 contains the definition for each type of team found in the questionnaire.<sup>5</sup> The definitions reveal that the teams differ along two primary dimensions: their area of focus and their level of autonomy. As for their focus, QITs/QCs and SDWTs concentrate on problems in their immediate work area, whereas CFTs draw members from a number of work areas. Of the three types of teams, SDWTs generally have the greatest level of autonomy. Across the fabs in our sample, QITs/QCs and CFTs are the *most* pervasive (11 fabs reported having such teams), with fabs reporting having 13 and 9 such teams respectively (median).

**Table 3D-6. Team Definitions**

Name of Team	Definition
Quality Improvement Teams/Quality Circles: (QITs/QCs)	Structured employee participation groups in which employees from a particular work area meet regularly to identify and suggest improvements to work-related problems.
Self-Directed Work Teams: (SDWTs)	The work group (in some cases acting without a supervisor) is responsible for work in its area of the fab, and it makes decisions about task assignments and work methods.
Cross-Functional Teams: (CFTs)	Structured employee participation groups in which employees from multiple work areas meet regularly to identify and suggest improvements to problems.

Given the nature of the teams, we predicted that SDWTs would have the greatest number of meetings a week, have compulsory membership, exist for more than a single project, and have the greatest level of autonomy for project selection and expenditures. As Table 3D-7 shows, the data support our predictions to some degree. However, managers play a larger role in SDWTs (as they do in all types of teams) than we anticipated.

**Table 3D-7. Characteristics of Teams**

	Team		
	QIT (n=11 Fabs)	SDWT (n=6 Fabs)	CFT (n=11 Fabs)
1) # of Meetings/Week	3	7	2
Max			
Min	0.25	0.5	0.25
Avg	1.0	1.9	0.8
2) Voluntary Membership?	8	2	7
Yes			
No	3	4	4
3) Single Project Only?	3	1	5
Yes			
No	8	5	6
4) Who Decides on Team's Projects?			
Total no. of fabs answering "Managers"	2	1	2
Total no. of fabs answering "Joint"	6	3	6
Total no. of fabs answering "Team"	3	2	3
5) Who Authorizes Team's Expenditures?			(n=10)
Total no. of fabs answering "Managers"	6	3	8
Total no. of fabs answering "Joint"	3	2	1
Total no. of fabs answering "Team"	1	0	1
Total no. of fabs answering "Other"	1	1	0
6) Are Managers or Supervisors Members?	9	4	10

Yes			
No	2	2	1

According to the data presented in Table 3D-7, CFTs and QITs exhibit very similar characteristics. The fabs in our sample emphasize both problem solving across multiple work areas *and* quality improvement activities in a single work area to a similar degree. The importance placed on cross-functional problem solving reflects an interesting feature of the semiconductor industry: The complicated interplay of processing steps requires that workers in different equipment areas communicate regularly.

Across the fabs in our sample, the three types of teams are very similar in terms of: size, meeting length, and use of structured problem-solving techniques. For all three types, the average number of members is approximately 10, with the average for SDWTs being the highest (13.3), and the average for CFTs being the lowest (7.5). An Asian fab reported having the largest teams, QITs/QCs with 30 members, while two other Asian fabs reported having the smallest teams, CFTs with 4 members. The meetings for all the teams in the sample last 1-2 hours. Only two fabs reported that their teams *do not* use formal problem-solving techniques: one Asian fab with QITs/QCs and one U.S. fab with SDWTs.

Table 3D-8 presents the share of team membership across the three primary occupations. Relative to operators and engineers, technicians have the *smallest* average membership share in QITs/QCs and CFTs. On average, operators constitute over 60% of the team members for both QITs and SDWTs, which is similar to their share of total headcount. Engineers constitute the highest average share of CFT membership, over 40%, which is triple their share of total headcount at many fabs in our sample. This high level of participation by engineers in CFTs reflects the technical challenges faced when problems span multiple work areas. Such problems require engineering expertise and leadership for resolution, since successful semiconductor manufacturing processes rely on the robust integration of process steps. The average percentage of technicians does not exceed 16% for any of the teams, which falls just below their average share of headcount.

**Table 3D-8. Team Membership by Occupation**

		QIT (n=11 Fabs)	SDWT (n=6 Fabs)	CFT (n=11 Fabs)
1) % Operators				(n=10)
	Max	100	100	70
	Min	0	10	0
	Avg	63.5	60.0	28.4
2) % Technicians		(n=10)		(n=10)
	Max	25	41	32
	Min	0	0	0
	Avg	10.0	12.7	15.2

3) % Engineers			(n=9)
	Max	100	10
	Min	0	0
	Avg	26.6	2.3
			6.89
			43.9

### 3D.5 Examples of Problem Solving

The previous sections have examined the primary mechanisms used in semiconductor manufacturing to improve the process flow: equipment maintenance, SPC, with coordinated problem solving through teams. Here we present examples of advanced problem solving from Japan, the U.S., and Korea. Advanced problem solving is done primarily by teams of engineers with only marginal input from technicians or operators, whose main contribution may be monitoring the process, collecting data, and running basic statistical analyses. We also observed lower-level problem solving by operators and technicians on problems relating directly to their jobs, such as routine maintenance for technicians and materials handling and machine operation for operators.

*Example from Japan:* In one company, the equipment maintenance department is expected to reach specific *kaizen* (improvement) goals, which tend to be “last year’s result plus alpha.” The examples here are from the photolithography group, which had the goal of improving the up-time on the steppers from 93.5% the previous year to 95%.

One group in photo determined that defects were caused by faulty nozzles used to apply develop compound onto the exposed wafers. While the standard develop nozzles on the develop tracks provided a uniform distribution of develop compound sprayed over the wafer surface, bubbles were discovered to be forming, which caused defects. They altered the configuration of the develop nozzles, allowing them to reduce the force and aeration of the spray. The modification eliminated the presence of bubbles and allowed for a 30% reduction in the consumption of develop compound. When asked if they showed this modification to the equipment maker, the engineer group leader replied, “Hell no!”

*Example from Korea:* One Korean company does in-line monitoring of machines and the process, and they also monitor probe yields at the end of the production line. Statistical analysis correlating yield losses with machines revealed an etch problem. The etch machines were found to be underetching. For a previous product, these machines had been used to do a trench etching that resulted in hardware damage. Although long etches like the trench etch are no longer done, the machines now had poor endpoint detection (*i.e.*, the etch stops “falsely” now) and this led to the underetching problem.

Two etch engineers formed the “yield improvement team” to do the analysis of the etchers. On a weekly basis, they combined data from the Poly Etch engineer, the Oxide Etch engineer, and one of the Metal Etch engineers to track the trend.

Their short-term solution was to add an inspect operation that measures the remaining oxide after etch. They discussed the problem with the vendor, who added a special operating instruction to the on-line manufacturing execution system, but this did not help and the vendor gave up. For the long term, they are evaluating a new recipe involving a fixed-time etch to replace the end-point based etch to see if it works satisfactorily. They hoped to have the new recipe finished within a month.

*Example from the U.S.:* At one U.S. company, yield improvement procedures are split into three cases: (1) reacting to a yield crises in which there are many wafers with low yields, indicating marginal equipment or process, (2) reacting to more than 5 wafers/lot with substandard yields, and (3) reacting to a yield excursion by a few wafers per lot or by an individual lot.

In case (1), the responsible device engineer monitoring the die yield will observe that a crisis has occurred. Operators will be instructed to put all lots on hold. A cross-functional team will be quickly put together to attend an afternoon meeting the same day. At the meeting, the device engineer will report his findings, and the team will discuss potential root causes. Experiments and/or lab analysis may be performed to prove identification of root cause (*e.g.*, examination). A containment plan will be devised and implemented. The team meets twice per day until the root cause is found.

One example of a case (1) procedure involved two steppers that were not fully printing. It turned out on one of the steppers, the lamp intensity had fallen too low, and on the other, there was too much lens drift. Both problems led to insufficient exposure. The device engineer figured it out from just going through the run cards to see the equipment commonalties. They changed the exposure energy to solve the problem. It took about 10-11 days.

### **3D.6 Skill Development and Career Ladders**

In this section, we turn to the important question of how high performing semiconductor companies develop the skills required by both front line workers and engineers for successful innovation on the shop floor. We will first examine how training is conducted and then turn to the question of how skill development is embedded in the employment system.

The semiconductor industry provides a lot of training across all occupations, from operators to engineers. This training is necessary because workers are involved in continuous problem solving in an industry that is continually introducing new processes or new products and is automating production facilities. The average number of days of initial training is similar across job categories, ranging from 21 to 27 days. The number of days of initial training is positively correlated with manufacturing performance for all three job categories.

After initial training, workers are receiving training about half the work time during the first year with the bulk of the training on the job. In subsequent years, about one-quarter of their work time is spent in training (Table 3D-9).

**Table 3D-9. Average Levels of Training Across Job Categories**

	Orientation Initial Training ( # Days)	First Year: Training or Learning New Skills (% of Time)		Subsequent Years: Training or Learning New Skills (% of Time)	
		OJT	Classroom	OJT	Classroom
Operators	27	40	5	16	6
Technicians	21	42	8	18	6
Engineers	26	39	8	12	10

No significant correlations were found between the amount of training during the first year or subsequent years and performance. However, there is a positive correlation between the use of both on-the-job training and classroom training and performance metrics across all job categories. Using OJT alone or classroom training alone is not correlated with respect improved performance. The results show that the type of training and how it is delivered rather than the time in training is important.

Training of technicians is more likely to be correlated with the performance metrics than training of operators and engineers as shown in Table 3D-10. We believe that this reflects the importance of machine up-time in determining machine productivity and the large variation in actual machine up-time observed across fabs.

**Table 3D-10. Correlation Between Specific Skill Training and Performance Metrics**

<i>TECHNICIANS</i>	Either Method of Training	Only On-The- Job Training	Only Classroom Training	Both Methods Of Training
Defect Density			H (+)	E,F (+)
Stepper Throughput				C,G,H,I,J,K (+)
Line Yield	A,D,E,F,H,J,K (+)		A (+)	F (+)
Cycle Time Per Layer				
Direct Labor Productivity	C,E,F,G,H,J,K (+)			C,G,J,K (+)

•Skill Legend: (A) basic skills, (B) basic science, (C) SPC, (D) company-specific orientation, (E) machine operation, (F) machine maintenance,, (G) teamwork/communication, (H) problem-solving methods, (I) design of experiments, (J) safety procedures, (K) cleanroom procedures.

•A '+' means there is a positive correlation. A '-' implies a negative correlation. Significance is at the 10% level.

Compared to operators in traditional manufacturing jobs, the operators in semiconductors oversee a highly technical process and undertake relatively complex technical tasks. Operators are involved in fairly high skilled procedures, including various types of SPC and equipment maintenance activities as demonstrated in Section 3D.3 above. Most operators are involved in data collection and monitoring, but the level of operator involvement declines as the difficulty of the task increases. The level of operator involvement in problem solving is usually limited to identifying the nature of the problem and notifying technicians or engineers. In a few fabs, operators are involved in performing some routine maintenance. Overall, operators perform tasks that require training and skill development. However, operators are still limited in their skill development and career growth, as well as wage growth, unless they become techs.

Two examples of career ladders for operator/technicians are shown in Table 3D-11. All production workers in the large Japanese semiconductor companies are on a career ladder that combines operator and technician tasks, training and skills. By age 40, Japanese electronics workers have technical skills and job tasks. In the U.S., the operator jobs are usually separated from the technician jobs,<sup>6</sup> and an operator does not necessarily (or usually) become a technician.

**Table 3D-11. Examples of Career Ladders in Two Semiconductor Firms**

<b>U.S. Firm:</b>	<b>Operator</b>	<b>Technician</b>
Entry Wage (hourly)	\$7	\$10
Top Wage	\$15	\$25
Top/Entry Pay Ratio	2.1	2.5
Approx. Time to Top	15 years	15 years

<b>Japanese Firm</b>	<b>Operator</b>
Entry Wage (monthly)	89,300 ¥
Top Wage	320,100 ¥
Top/Entry Pay Ratio	3.6
Approx. Time to Top	20 + years

However, most fabs provide the opportunity for an operator to move up to a technician job. To do this, the operator typically must return to school to earn an AA degree in electronics, since fewer than 10% of operators have AA degrees. They also must take some home study courses as well as undertake specific company-provided training (including on the job training in certain processes.) The requirements are rigorous and require a lot of nonpaid time and commitment. At the U.S. company shown in the example, which encourages internal promotion, only one-third of the operators become technicians and one-half of the technicians were promoted from operator. For those operators who do become technicians at this U.S. company, their career ladders looks like the Japanese career ladder, which runs about 20 plus years and includes wages increasing 3.6 times.

Korean fabs provide an interesting contrast to both the Japanese and U.S. cases, since operator jobs are strictly segmented from technician jobs. Women, who live and work at the company for only three to five years before quitting to get married, are operators; men, who usually have long careers with the company, are technicians (as well as engineers and managers).

In the U.S., hourly earnings in the semiconductor industry have increased as the importance of technicians has increased (see chapter 5). However, average earnings (\$14.50 in 1994) are still low compared to UAW production and craft workers, who earned \$18.28 and \$21.44, respectively, in the Big Three automobile companies in 1994.<sup>7</sup>

American semiconductor companies increased employment in the U.S. relative to employment offshore since 1991, so that U.S. employment exceeded offshore employment in 1994 for the first time during the 1978 through 1994 period.<sup>8</sup> Overall, the outlook for employment, especially technicians and engineers, is strong even in the presence of increasing automation. Although there is the potential for long career ladders for non-college graduates, the upgrading requires a technical education pursued outside of work to complement work-based training. The semiconductor industry pays relatively lower wages than unionized manufacturing in the U.S. but above average wages for all manufacturing, which has lower skill requirements.

### **3D.7 Conclusion**

This study has found that companies can foster innovation on the shop floor through various types of employment systems, which reflect differences in social structures and goals. However, some approaches seem to be more effective than others in terms of company performance. Even though labor costs rarely exceed 10% of total costs in semiconductor manufacturing, human creativity and involvement in problem solving are necessary for success. Our findings can be summarized under three categories:

#### ***3D.7a Creativity versus Control***

- A trade-off exists between fostering individual creativity and controlling innovation, especially for engineers involved in the transfer of new technology to high-volume fabs. Organization of process transfer activities both accommodates and requires the differences found across the U.S. and Japanese HR systems. These differences have the profound effect of determining innovation, diffusion, and control of the process. Precisely those structures of the Japanese firm that support team-based learning and problem solving impose constraints on individual initiative and autonomy; for example, relying on team activities for developing skills and for reaching specific goals increases an individual's dependence on other team members for his own personal success. Precisely those structures of the American firm that support individual creativity and breakthroughs impose problems of control over the process; for example, a system that promotes individual achievements raises potential problems of coordinating problem solving both within and across fabs. Autonomy and creativity are highly

prized at USTech in development, but not in manufacturing. A consensus approach is practiced at JapanTech, and teamwork and stability are highly prized.

- Designating the level of process maturity required for transfer from development to a manufacturing fab determines the role of development and manufacturing engineers in creating new production processes. USTech depends on development engineers for creative solutions to processing issues while trying to control the creative impulses of manufacturing engineers. JapanTech depends less on its development engineers and more on the manufacturing engineers for creative approaches, since process modifications and improvements are made at the fab by the manufacturing engineers.
- Although engineers at both companies prefer development work to mundane tasks such as documenting modifications and calibrating equipment, this problem seems to be more widespread at JapanTech. At JapanTech, engineers typically begin work with a B.S. degree, and initially are not specialized in development or manufacturing. JapanTech's engineers (excluding those at the Central Research Labs) rotate among development and fabrication tasks. USTech's engineers are more specialized, leading to a clearer division of work assignments. Their work reflects their education with the development and research engineers likely to have an advanced degree while the manufacturing engineers are hired with B.S. degrees.

### ***3D.7b Problem Solving and Coordination***

- A trade-off exists between supporting information sharing for joint problem solving and supporting individual creativity in problem solving. The Japanese human resource system has highly developed mechanisms to support intrafirm knowledge creation and sharing (*i.e.*, the joint sharing of knowledge and skills among employees within a team and across groups). The U.S. human resource system is better at structuring and rewarding individual, as opposed to group, initiative and endeavors.
- Overall, equipment maintenance and SPC activities exhibit a greater degree of variation in human resources practices across the fifteen fabs in our sample than do the team characteristics. However, fabs that use teams to coordinate problem solving and enhance knowledge sharing across job categories improve their ability to implement enduring solutions to processing problems.

### ***3D.7c Career Ladders and Work Organization***

- Operators/technicians face a more defined career ladder with skill development and wage growth in Japan than in the U.S. or Korea. Career ladders create incentives for nonprofessional workers to develop skills, to engage in problem solving, and to remain with the company. Career ladders also improve access to higher earnings.
- For engineers, JapanTech's job assignment and pay system is heavily influenced by tenure, although performance becomes more important after an engineer has worked at the company more than ten years and after he reaches management. USTech's job

assignment and pay system is heavily influenced by performance and so there is much more variation in career paths and earnings observed among its engineers.

- The complexity of the production process requires both classroom training and hands-on learning in the fab. Even with extensive work experience, operators are rarely promoted into the technician job category. Likewise technicians are rarely promoted into the engineer job category without additional schooling.

The findings presented in this paper support the hypothesis posited above: A high performing HR system in a high-tech setting can be created by the effective management of engineering talent, the involvement of line workers in problem solving, coordinated troubleshooting on the shop floor, and the construction of career ladders that integrate worker development and compensation. Our results indicate that when employee involvement in problem solving is separated from skill development, the resulting HR system has lower performance. Successful employee involvement must integrated skill development into problem solving and appears to be reinforced by career ladders within the firm.

## APPENDIX 1. Equipment Maintenance Activities

High-Level (weight 3)	Medium-Level (weight 2)	Low-Level (weight 1)
a. Perform Annual Equipment Maintenance  (Annual Mnt)	a. Produce Checklists for Inspecting Equipment  (Check lists)	a. Daily or Weekly Inspection (Inspect.)
b. Know Relation between Equipment Precision and Product Quality (Prec-Prod /Qual)	b. Perform Weekly Equipment Maintenance (Weekly Mnt)	b. Document Equipment Breakdowns (Doc. Bkdns)
c. Ability to Repair Equipment (Repair)	c. Perform Monthly Equipment Maintenance (Monthly Mnt)	c. Able to Recognize and Document Equipment Abnormalities (Recog/Doc)
d. Perform Analyses of Equipment Breakdowns (Bkdn Analysis)	d. Perform Use-Based Equipment Maintenance (Use-B Mnt)	d. Perform Daily Equipment Maintenance (Daily Mnt)
e. Modify Equipment to Improve Process Yield (Modify-PR)	e. Draft Equipment Clean/Maint. Procedures for Routine Activities (Draft Procs)	e. Clean and/or Lubricate Equipment (Clean/Lube)
f. Modify Equipment for Easier Inspection and Maintenance (Modify-Inspec)	f. Attend Equipment Inspec./Maint. Classes Offered by Vendor (Ven Classes)	
g. Analyze and Improve Equipment Clean/Maint. Activities  (Improve Clean)	g. Ownership of Individual Equipment or Equipment Type (Ownership)	
h. Find Ways to Reduce Equipment Set-Up/Adjustment Time (Reduce Set-up)	h. Knowledge of Function and Structure of Equipment (Fn & Struc)	

**APPENDIX 1. (Continued.)**

<b>High-Level (weight 3)</b>	<b>Medium-Level (weight 2)</b>	<b>Low-Level (weight 1)</b>
i. Find Ways to Increase the Life Span of Equipment (Increase-Life)	i. Ability to Replace Simple Equipment Parts (Replace Parts)	
j. Find Ways to Reduce Unexpected Equipment Breakdowns (Reduce Bkdns)	j. Authorized to Take Corrective Action on Equipment (Correc Action)	
k. Find Ways to Reduce Equipment Particle Generation (Reduce Partcl)	k. Train Peers in Equipment Inspection, Maint. or Cleaning Procedures (Train Peers)	
l. Set Specific Goals for Reducing Equipment Non-Operating Time (Goals Non-Op)	l. Train Subordinates in Equipment Inspection, Maint. or Cleaning Procedures (Train Subords)	
m. Set Specific Goals for Defect Reduction (Goals Defect)		

## APPENDIX 2. SPC Activities

High-Level (weight 3)	Medium-Level (weight 2)	Low-Level (weight 1)
a. Plan Action based on Control Charts (Plan Actions)	a. Cp and Cpk (Cp, Cpk)	a. X-Bar, R (X-Bar, R)
b. Cause-and-Effect or "Fishbone" Diagrams (Fishbone)	b. Flow Charts and/or Histograms (Flow/Histograms)	b. X-Bar, S (X-Bar, S)
c. Deming Cycle (plan-do-check-act) (Deming)	c. Brainstorming (Brainstorming)	c. p-charts (P-Charts)
d. Pareto-Problem ID (Pareto-Prob ID)	d. Train Others in SPC Methods (Train Others)	d. Manual Control Charts (Control Chart-Man)
e. Pareto-Cost (Pareto-Cost)		e. Quality Data-Computer (Quality Data-Comp)
f. QC or QI story (QC or QI Story)		f. Manual Gather Data (Gather Data-Man)
g. Communicate with Customers (Comm. Cust.)		
h. Communicate with Suppliers/Vendors (Comm. Sup/Ven)		

<sup>1</sup> We are grateful to our colleagues in the CSM program for their input. In particular, we would like to thank Neil Berglund, Dave Bowen, David Mowery, Nile Hatch, and Dan Rascher. The fab-level data used in this study was collected by the CSM Project team. See Leachman, Robert C. and D. A. Hodges, 1996, "Benchmarking Semiconductor Manufacturing," IEEE Transactions on Semiconductor Manufacturing, Vol 9 No 2, p. 158-169 (May, 1996); Robert Leachman, ed., *The Competitive Semiconductor Manufacturing Survey: Third Report on Results of the Main Phase* (Report CSM-31), chapter 2, August 1996; and Clair Brown, ed., *The Competitive Semiconductor Manufacturing Human Resources Project: Second Interim Report*, CSM-32, September 1996.

<sup>2</sup> Brown, "Managing Creativity and Control in Innovation" in Report CSM -32 explores innovation by engineers in development by USTech and JapanTech. Appleyard, "How Does Knowledge Flow? Inter-

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Firm Patterns in the Semiconductor Industry” in Report CSM-32 analyses how engineers from the two countries receive and share technical information across company lines.

<sup>3</sup> In addition to the CSM main study data referenced in footnote 1, this research is based upon several field work trips to both USTech and JapanTech where in-depth interviews with over a dozen engineers and managers at each company were conducted.

<sup>4</sup> For a detailed documentation and analysis of the Japanese and American employment and wage system, see Clair Brown, Yoshi Nakata, Michael Reich, and Lloyd Ulman, *Work and Pay in United States and Japan*, Oxford University Press, 1997.

<sup>5</sup> Definitions are courtesy of Edward E. Lawler, School of Business Administration, University of Southern California.

<sup>6</sup> In the 28 fabs studied, we observed only two U.S. fabs that combined operator and technician into one job category.

<sup>7</sup> Summary of the UAW-Ford national contract, Bureau of National Affairs, Inc. *Daily Labor Reporter*, Washington D.C., No. 184, September 24, 1993. The hourly wage for janitors was \$17.85. Ford workers also earned a performance and Christmas bonus, usually between \$2000 and \$2300.

<sup>8</sup> Semiconductor Industry Association, *SIA Annual Databook: 1995*, 1995.